WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a cell array having a plurality of memory cells,

each of said memory cells including:

first and second switch transistors connected in series between a first bit line for a write system and a second bit line for a read system; and

a capacitor for storing data, connected to a connection node at which the first and second switch transistors are tied;

the first and second switch transistors having control terminals connected to a first word line for a write system and a second word line for a read system respectively;

an address holding circuit for receiving and holding an address signal supplied from an outside of said semiconductor memory device;

a first determination circuit for comparing a refresh address with a row address, selected according to a control signal commanding a read/write operation, between row addresses of a read address signal and a write address signal held in said address holding circuit to determine whether the refresh address matches the selected row address or not; and

a control unit for performing control so that

when a mismatch is detected as a result of the determination by said first determination circuit, the read or write operation and a refresh operation are performed in parallel, wherein the read or write operation is performed using the word line and the bit line for one of said read and write systems for the memory cell selected by the read or write address

signal, while the refresh operation is performed using the word line and the bit line for the other of said read and write systems for the memory cell selected by the refresh address signal and a sense amplifier for the other of said read and write systems, and

when the match is detected as the result of the determination by said first determination circuit, the refresh operation is inhibited and the read or write operation using the word line and the bit line for said one of said read and write systems for the memory cell selected by the read or write address signal is performed.

2. A semiconductor memory device comprising a cell array having a plurality of memory cells,

each of said memory cells including:

first and second switch transistors connected in series between a first bit line for a write system and a second bit line for a read system; and

a capacitor for storing data, connected to a connection node at which the first and second switch transistors are tied;

the first and second switch transistors having control terminals connected to a first word line for a write system and a second word line for a read system respectively;

an address holding circuit for receiving and holding a row address of an address signal for write supplied from an outside of said semiconductor memory device;

a first determination circuit for comparing a refresh address with the row address of the address signal for write held in said address

holding circuit to determine whether the refresh address matches the row address for the address signal for write or not; and

a control unit for performing control so that

when a mismatch is detected as a result of the determination by said first determination circuit, a write operation and a refresh operation are performed in parallel, wherein the write operation is performed using the word line and the bit line for a write system for the memory cell selected by the address signal for write, while the refresh operation is performed using the word line and the bit line for a read system for the memory cell selected by the refresh address and a sense amplifier for a read system, and

when the match is detected as the result of the determination by said first determination circuit, the refresh operation is inhibited, and the write operation is performed.

3. The semiconductor memory device according to claim 1, further comprising:

a second determination circuit for determining whether the address signal supplied to said semiconductor memory device from the outside of said semiconductor memory device matches the write address signal held in said address holding circuit;

a data holding circuit for holding data for write; and

a control circuit for performing control so that when a input read address signal matches the write address signal held in said address holding circuit as a result of the determination by said second determination circuit, data held in the data holding circuit is output from

a readout data output terminal.

4. The semiconductor memory device according to claim 2, further comprising:

a second determination circuit for determining whether the address signal supplied to said semiconductor memory device from the outside of said semiconductor memory device matches the write address signal held in said address holding circuit;

a data holding circuit for holding data for write; and

a control circuit for performing control so that when a read address signal matches the write address signal held in said address holding circuit as a result of the determination by said second determination circuit, data held in the data holding circuit is output from a readout data output terminal.

5. The semiconductor memory device according to claim 1, wherein said first determination circuit compares the refresh address with the row address of the write address signal to determine whether the refresh address matches the row address of the write address signal before a cycle of performing the write operation to said cell array is started.

6. The semiconductor memory device according to claim 2, wherein said first determination circuit compares the refresh address with the row address of the write address signal to determine whether the refresh address matches the row address of the write address signal before a cycle of performing the write operation to said cell array is started.

7. The semiconductor memory device according to claim 1, wherein said address holding circuit comprises:

a first address holding circuit for holding the row address of the write address signal (referred to as a "row address for a write system") input from an address terminal, delaying the row address for a write system by a predetermined number of write cycles to output the delayed row address, and outputting the row address for the read address signal (referred to as a "row address for a read system") input from said address terminal without delay; and

a second address holding circuit for holing a column address of the write address signal (referred to as a "column address for a write system") input from said address terminal, delaying the column address for a write system by the predetermined number of write cycles to output the delayed the column address, and outputting a column address of the read address signal(referred to as a "column address for a read system") input from said address terminal without delay;

wherein said first address holding circuit comprises at least one match detection circuit for determining whether the row address for the address signal input from said address terminal matches the row address of the write address signal held in said first address holding circuit; and

wherein said second address holding circuit comprises at least one match detection circuit for determining whether the column address of the address signal input from said address terminal matches the column address of the write address signal held in said second address holding circuit.

8. The semiconductor memory device according to claim 2, wherein said address holding circuit comprises:

a first address holding circuit for holding the row address of the write address signal (referred to as a "row address for write") input from an address terminal, delaying the row address for write by a predetermined number of write cycles to output the delayed row address, and outputting a row address of a read address signal (referred to as a "row address for read") input from said address terminal without delay; and

a second address holding circuit for holding a column address of the write address signal(referred to as a "column address for write") input from said address terminal, delaying the column address for write by the predetermined number of write cycles to output the delayed row address, and outputting a column address of the read address signal (referred to as a "column address for read") input from said address terminal without delay;

wherein said first address holding circuit comprises:

a first match detection circuit for comparing the row address for write with the refresh address to determine whether the row address for write matches the refresh address before delaying the row address for write by the predetermined number of write cycles for supply; and

at least one second match detection circuit for determining whether the row address for the address input from said address terminal matches the row address of the write address held in said first address holding circuit; and

wherein

said second address holding circuit comprises:

at least one match detection circuit for determining whether the column address for the address input from said address terminal matches the column address for the write address held in said second address holding circuit; and

said first match detection circuit in said first address holding circuit constitutes said first determination circuit.

9. The semiconductor memory device according to claim 8, wherein said first address holding circuit comprises:

a latch circuit of an input stage, for sampling row address signal of an address signal input from said address terminal in response to an internal clock signal; and

a write address holding circuit comprising a plurality of latch circuits connected in cascade, each of said latch circuits sampling a signal at an input terminal thereof to output the sampled signal from an output terminal thereof in response to a clock signal for write control activated during a write cycle, a first stage of said latch circuits receiving an output signal of said latch circuit of said input stage at the input terminal thereof, and the output signal of said latch circuit of said input stage being delayed by the predetermined number of write cycles and output from the output terminal of a last stage of said latch circuits;

wherein said first match detection circuit compares an output signal of a stage of said latch circuits preceding said last stage in said write address holding circuit with the refresh address to determine whether the output signal matches the refresh address or not;

wherein said second match detection circuit compares the output

signal of said stage of said latch circuits preceding said last stage in said write address holding circuit with the output signal of said latch circuit in said input stage to determine whether the output signals match with each other or not; and wherein

said semiconductor memory device further comprises:

a selection circuit for receiving an output of said latch circuit in said input stage and the refresh address, selecting the refresh address when a refresh control signal as a selection control signal is activated, and selecting the output of said latch circuit in said input stage when the refresh control signal is deactivated.

10. The semiconductor memory device according to claim 9, further comprising:

a control circuit for performing control so that when there is even one unmatching bit between the row address for write held in said first address holding circuit and the refresh address, the refresh control signal is activated, and a read or write operation and the refresh operation are performed in parallel, the read or write operation being performed using the word line and the bit line for one of said read and write systems, selected by the address for said read or write system, the refresh operation being performed using the word line and the bit line for the other of said read and write systems selected by the refresh address and a sense amplifier for the other of said read and write systems.

11. The semiconductor memory device according to claim 7, further comprising:

a first selection circuit for receiving the row addresses for said write and read systems output from said first address holding circuit, selecting and outputting the row address for read supply when the control signal commanding the read/write operation indicates a read, and selecting and outputting the row address for write when the control signal indicates a write;

an address comparison circuit for comparing the row address output from said first selection circuit with the refresh address output from a refresh address generation circuit;

a read/write and refresh control circuit for outputting a refresh control signal for a read system and a refresh control signal for a write system for controlling a refresh using one of the addresses for said read and write systems according to a result of the comparison from said address comparison circuit and the control signal commanding the read/write operation;

a second selection circuit for receiving the row address for write output from said first address holding circuit and the refresh address output from said refresh address generation circuit, receiving the refresh control signal for a write system from said read/write and refresh control circuit as a selection control signal, selecting and outputting the refresh address when the refresh control signal for a write system is activated to indicate the refresh, and selecting and outputting the row address for write when the refresh control signal for a write system is deactivated;

a third selection circuit for receiving the row address for read

output from said first address holding circuit and the refresh address from said refresh address generation circuit, receiving the refresh control signal for a read system from said read/write and refresh control circuit as the selection control signal, selecting and outputting the refresh address when the refresh control signal for a read system is activated to indicate the refresh, and selecting and outputting the row address for read for supply when the refresh control signal for a read system is deactivated;

a first X decoder receiving and decoding the row address from said second selection circuit for selecting the first word line for a write system;

a second X decoder receiving and decoding the row address from said third selection circuit for selecting the second word line for a read system;

a first Y decoder receiving and decoding the column address for write output from said second address holding circuit, activation of said first Y decoder being controlled by the refresh control signal for a write system from said read/write and refresh control circuit;

a first sense amplifier connected to the first bit line for a write system, activation of said first sense amplifier being controlled by the refresh control signal for a write system from said read/write and refresh control circuit;

a second Y decoder for receiving the column address for read output from said second address holding circuit, activation of said second Y decoder being controlled by the refresh control signal for a

read system from said read/write and refresh control circuit; and

a second sense amplifier connected to the second bit line for a read system, activation of said second sense amplifier being controlled by the refresh control signal for a read system from said read/write and refresh control circuit.

12. The semiconductor memory device according to claim 8, further comprising:

a read/write and refresh control circuit for outputting a refresh control signal for a read system and a control signal controlling an operation of said write system according to a result of the comparison from said match detection circuit of said first address holding circuit constituting said first determination circuit and a control signal commanding a read operation or the write operation;

a first X decoder receiving and decoding the row address for write output from said first address holding circuit for selecting the first word line for a write system;

a second X decoder receiving and decoding the row address output from a selection circuit of said first address holding circuit for selecting the second word line for a read system;

a first Y decoder receiving and decoding the column address for write output from said second address holding circuit;

a second Y decoder receiving and decoding the column address for read output from said second address holding circuit;

a first sense amplifier connected to the first bit line for a write system; and

a second sense amplifier connected to the second bit line for a read system, activation of said second sense amplifier being controlled by the refresh control signal for a read system from said read/write and refresh control circuit.

13. The semiconductor memory device according to claim 1, wherein said semiconductor memory device comprises:

a timer generating a trigger signal for defining a refresh cycle; and

a refresh address generation circuit for generating the refresh address based on the trigger signal from said timer,

wherein said semiconductor memory device is interface compatible with a static random access memory of a clock synchronous type.

14. The semiconductor memory device according to claim 2, wherein said semiconductor memory device comprises:

a timer generating a trigger signal for defining a refresh cycle; and

a refresh address generation circuit for generating the refresh address based on the trigger signal from said timer,

wherein said semiconductor memory device is interface compatible with a static random access memory of a clock synchronous type.

15. The semiconductor memory device according to claim 11, wherein said first and second X decoders are disposed to be opposite to each other with respect to said cell array interposed therebetween; and wherein said first and second sense amplifiers are disposed to be

opposite to each other with respect to said cell array interposed therebetween.

16. The semiconductor memory device according to claim 12, wherein said first and second X decoders are disposed to be opposite to each other with respect to said cell array interposed therebetween; and wherein said first and second sense amplifiers are disposed to be opposite to each other with respect to said cell array interposed therebetween.

17. The semiconductor memory device according to claim 7, wherein said first and second write address holding circuits respectively comprises an address holding circuit constituted from pairs of latch circuits connected in cascade, each of said pairs of latch circuits sampling data at falling and rise edges of a clock signal for write control, a number of said pairs being equivalent to the predetermined number of write cycles.

18. The semiconductor memory device according to claim 8, wherein said first and second write address holding circuits respectively comprises an address holding circuit constituted from pairs of latch circuits connected in cascade, each of said pairs of latch circuits sampling data at falling and rise edges of a clock signal for write control, a number of said pairs being equivalent to the predetermined number of write cycles.

19. The semiconductor memory device according to claim 11, wherein the semiconductor memory device is interface compatible with a clock synchronous type static random access memory.

20. The semiconductor memory device according to claim 12, wherein the semiconductor memory device is interface compatible with a clock synchronous type static random access memory.

21. The semiconductor memory device according to claim 1, further comprising:

a control circuit for performing control so that over a plurality of clock cycles, the selected word line is activated, and data writing to the memory cell or data reading from the memory cell is performed.

22. The semiconductor memory device according to claim 2, further comprising:

a control circuit for performing control so that over a plurality of clock cycles, the selected word line is activated, and data writing to the memory cell or data reading from the memory cell is performed.

23. The semiconductor memory device according to claim 21, wherein two data items are input/output from a data input terminal/data output terminal in one clock cycle at rise and fall edges of a clock;

the semiconductor memory device comprises:

a parallel-to-serial conversion circuit for converting four data items read in parallel to four serial data items in two clock cycles; and

a delay control circuit for controlling a delay in a timing of the clock supplied to said parallel-to-serial conversion circuit; and

a timing of output from said data output terminal is in synchronization with the clock signal.

24. The semiconductor memory device according to claim 22, wherein two data items are input/output from a data input terminal/data output

terminal in one clock cycle at rise and fall edges of a clock;

the semiconductor memory device comprises:

a parallel-to-serial conversion circuit for converting four data items read in parallel to four serial data items in two clock cycles; and

a delay control circuit for controlling a delay in a timing of the clock supplied to said parallel-to-serial conversion circuit; and

a timing of output from said data output terminal is in synchronization with the clock signal.

25. The semiconductor memory device according to claim 1, further comprising:

a control circuit for performing control so that when the mismatch is detected as the result of the determination by said first determination circuit, the read or write operation and the refresh operation are simultaneously started.

26. The semiconductor memory device according to claim 2, further comprising:

a control circuit for performing control so that when the mismatch is detected as the result of the determination by said first determination circuit, the write operation and the refresh operation are simultaneously started.

27. A semiconductor memory device adapted to have an interface compatible with a static random access memory, comprising:

a cell array including a plurality of DRAM(dynamic random access memory) cells, each having a port for a write system and a port for a read system;

an address holding circuit for holding an externally input address;

a refresh address generation circuit for generating a refresh address; and

a comparator circuit for comparing the refresh address output from said refresh address generation circuit with the address held in said address holding circuit; and

a control circuit for performing control so that, when the comparison result indicates that the refresh address does not match the address, a read or write operation using one of the ports for the write and read systems of selected one of said DRAM cells and a refresh operation using the other of the ports for the write and read systems are performed in parallel, and when the comparison result indicates that the refresh address matches the address, the refresh operation is stopped.

28. The semiconductor memory device according to claim 27, wherein the semiconductor memory device is adapted for the refresh operation to be performed using the port for the read system;

wherein the comparator circuit compares the refresh address with the address for write held in said address holding circuit; and

wherein the control circuit performs control so that, when the comparison result indicates that the refresh address does not match the address for write, a write operation using the port for the write system of selected one of said DRAM cells and a refresh operation using the port for the read system are performed in parallel, and when the comparison result indicates that the refresh address matches the address for write, the refresh operation is stopped.

29. The semiconductor memory device according to claim 27, wherein the semiconductor memory device is interface compatible with a QDR (Quad Data Rate) SRAM (Static Random Access Memory).

30. A semiconductor memory device comprising:

a data input buffer having at least an input terminal for receiving a plurality of data signals serially supplied to the semiconductor memory device from an outside of the semiconductor memory device;

a first converter, receiving a plurality of data signals serially output from the data input buffer, for applying serial to parallel conversion to the serially received data signals to derive and output parallel data signals;

a first register, receiving the parallel data signals output in parallel from the first converter, for sampling the parallel data signals;

an address register for sampling and holding an input address signal supplied to the semiconductor memory device from the outside of the semiconductor memory device;

a memory cell array having a plurality of memory cells, said memory cell array being so adapted to receive and store the parallel data signals output from said first register in the memory cells associated with the input address signal output from said address register in a write operation and to output data, which are read from the memory cells associated with the input address signal received from said address register, as parallel data signals in a read operation, each of said memory cells being a dual port memory cell which needs a refresh operation in order to hold data stored therein;

a multiplexer, receiving the parallel data signals output from said memory cell array and said parallel data signals output from said first register, as two inputs, for selecting and outputting one of two inputs;

a second converter, receiving the parallel data signals output from said multiplexer, for applying parallel to serial conversion to the received parallel data signals to output a resultant plurality of data signals serially;

a data output buffer having at least an input terminal for receiving the plurality of data signals serially output from said second converter and an output terminal for outputting the received data signals serially to the outside of the semiconductor memory device;

a refresh address generator for generating a refresh address signal;

an address comparator, receiving the refresh address signal output from the refresh address generator with the input address signal held in the address register for comparing the refresh address signal with the input address signal to output a comparison result indicating whether there is a match between the refresh address signal and the input address signal or not; and

a control circuit for performing control so that refresh operation as to the dual port memory cell associated with the refresh address signal and a read or write operation as to the dual port memory cell associated with the input address signal are executed in parallel, when the comparison result output from the comparator indicates a mismatch between the refresh address signal and the address signal held in the

address register.

31. The semiconductor memory device according to claim 30, wherein said control circuit performs control to inhibit the refresh operation as to the dual port memory cell associated with the refresh address signal when the comparison result output from the comparator indicates a match between the refresh address signal and the address signal held in the address register.

32. The semiconductor memory device according to claim 30, further comprising a circuit for comparing the input address signal for read and the address signal for write held in the address register; wherein said multiplexer selects and outputs the parallel data signals output from the first register when the input address signal matches for read and the address signal for write held in the address register.

33. A semiconductor memory device comprising:

a data input buffer having at least an input terminal for receiving a plurality of data signals serially supplied to the semiconductor memory device from an outside of the semiconductor memory device, said plurality of data signals including at least two consecutive data signals, one of which corresponds to a rising edge of a clock signal for use of synchronized operation and other of which corresponds to a falling edge of the clock signal;

a first converter, receiving a plurality of data signals serially output from the data input buffer, for applying serial to parallel conversion to the serially received data signals to derive and output parallel data signals;

a first register, receiving the parallel data signals output in parallel from the first converter, for sampling the parallel data signals;

an address register, receiving an input address signal supplied to the semiconductor memory device from the outside of the semiconductor memory device, for sampling and holding the input address signal by using a rising edge and/or a falling edge of the clock signal;

a first control circuit for generating a read/write control signal commanding a read/write operation ;

a memory cell array having a plurality of memory cells, said memory cell array being so adapted to receive and store the parallel data signals output from said first register in the memory cells associated with the input address signal output from said address register via a write bus when the read/write control signal indicate a write operation and to output data, which are read from the memory cells associated with the input address signal received from said address register, as parallel data signals to a read bus when the read/write control signal indicate a read operation, each of said memory cells being a dual port memory cell which needs a refresh operation in order to hold data stored therein;

a multiplexer, receiving from the read bus the parallel data signals read from said memory cell array and said parallel data signals output from said first register, as two inputs, for selecting and outputting one of two inputs;

a second converter, receiving the parallel data signals output from said multiplexer, for applying parallel to serial conversion to the received parallel data signals to output a resultant plurality of data

signals serially;

a data output buffer having at least an input terminal for receiving the plurality of data signals serially output from said second converter and an output terminal for outputting the received data signals serially to the outside of the semiconductor memory device;

a refresh address generator for generating a refresh address signal;

an address comparator, receiving the refresh address signal output from the refresh address generator with the input address signal held in the address register for comparing the refresh address signal with the input address signal to output a comparison result indicating whether there is a match between the refresh address signal and the input address signal or not; and

a second control circuit for performing control so that refresh operation as to the dual port memory cell associated with the refresh address signal and a read or write operation as to the dual port memory cell associated with the input address signal are executed in parallel, when the comparison result output from the comparator indicates a mismatch between the refresh address signal and the address signal held in the address register.

34. The semiconductor memory device according to claim 32, wherein said second control circuit performs control to stop the refresh operation as to the dual port memory cell associated with the refresh address signal when the comparison result output from the comparator indicates a match between the refresh address signal and the address signal held in

the address register.

35. The semiconductor memory device according to claim 33, further comprising a circuit for comparing the input address signal for read and the address signal for write held in the address register; wherein said multiplexer selects and outputs the parallel data signals output from the first register when the input address signal matches for read and the address signal for write held in the address register.

36. A method of controlling a semiconductor memory device which comprises:

a cell array having a plurality of memory cells,

each of said memory cells including:

first and second switch transistors connected in series between a first bit line for a write system and a second bit line for a read system; and

a capacitor for storing data, connected to a connection node at which the first and second switch transistors are tied;

the first and second switch transistors having control terminals connected to a first word line for a write system and a second word line for a read system respectively; and

an address holding circuit for holding an address input from an outside of said semiconductor device;

the method comprising the steps of:

comparing a refresh address with a row address selected according to a control signal commanding a read/write operation between row addresses of read and write addresses held in said address

holding circuit to determine whether the refresh address matches the row address for the address or not;

performing control so that when a mismatch is detected as a result of the determination, the read or write operation and a refresh operation are performed in parallel, wherein the read or write operation is performed using the word line and the bit line for one of said read and write systems for the memory cell selected by the read or write address, while the refresh operation is performed using the word line and the bit line for the other of said read and write systems for the memory cell selected by the refresh address and a sense amplifier for the other of said read and write systems; and

performing control so that when the match is detected as the result of the determination, the refresh operation is inhibited, and the read or write operation using the word line and bit line for said one of said read and write systems for the memory cell selected by the read or write address is performed.

37. A method of controlling a semiconductor memory device which comprises:

a cell array having a plurality of memory cells,

each of said memory cells including:

first and second switch transistors connected in series between a first bit line for a write system and a second bit line for a read system; and

a capacitor for storing data, connected to a connection node at which the first and second switch transistors are tied;

the first and second switch transistors having control terminals connected to a first word line for a write system and a second word line for a read system respectively; and

an address holding circuit for holding a row address for an address for writing input from an outside of said semiconductor device;

said method comprising the steps of:

comparing a refresh address with the row address for the address for write held in said address holding circuit to determine whether the refresh address matches the row address for the address for write or not;

performing control so that when a mismatch is detected as a result of the determination, a write operation and a refresh operation are concurrently performed during a same cycle, wherein the write operation is performed using the word line and the bit line for a write system for the memory cell selected by the address for write, while the refresh operation is performed using the word line and the bit line for a read system for the memory cell selected by the refresh address and a sense amplifier for a read system; and

performing control so that when the match is detected as the result of the determination, the refresh operation is inhibited, and the write operation is performed.

38. The method according to claim 36, further comprising the steps of:

determining whether the address supplied from said outside of said semiconductor memory device matches the write address held in said address holding circuit; and

performing control so that when an input read address matches the

write address held in said address holding circuit, data held in a data holding circuit is read and output from a data output terminal.

39. The method according to claim 37, further comprising the steps of:

determining whether the address supplied from said outside of said semiconductor memory device matches the write address held in said address holding circuit; and

performing control so that when an input read address matches the write address held in said address holding circuit, data held in a data holding circuit is read and output from a data output terminal.

40. The method according to claim 37, further comprising the step of:

comparing the refresh address with the row address of the write address to determine whether the refresh address matches the row address of the write address before a cycle of performing the write operation to said cell array is started.

41. A method of controlling a semiconductor memory device including a cell array comprising a plurality of DRAM (dynamic random access memory) cells, each having a port for a write system and a port for a read system, said semiconductor memory device having an auto refresh function and being interface compatible with a static random access memory,

said method comprising the steps of:

storing and holding an externally input address in address holding circuit;

comparing a refresh address output from refresh address generation circuit with the address held in said address holding circuit;

performing control so that when the comparison result indicates that the refresh address does not match the address, a read or write operation using one of the ports for the write and read systems of selected one of said DRAM cells and a refresh operation using the other of the ports for the write and read systems are performed in parallel; and

performing control so that when the comparison result indicates that the refresh address matches the address, the refresh operation is stopped.

42. The method according to claim 36, wherein

in the step of performing control so that the read or write operation and the refresh operation are in parallel performed, control is performed so that the read or write operation and the refresh operation are simultaneously started.

43. The method according to claim 37, wherein

in the step of performing control so that the write operation and the refresh operation are performed in parallel, control is performed so that the write operation and the refresh operation are simultaneously started.

44. A method of controlling a semiconductor memory device which comprises: a cell array having a plurality of memory cells, each of which needs a refresh operation to hold data stored therein;

an address holding circuit for holding an address supplied from an outside of said semiconductor memory device; and

a data holding circuit for holding data supplied from an outside of said semiconductor memory device,

said method comprising the steps of:

storing the externally supplied address and the externally supplied data in said address holding circuit and said data holding circuit, respectively;

comparing a row address for the address for write held in said address holding circuit with a refresh address;

controlling so that a write operation for writing the data held in said data holding circuit to said cell array and a refresh operation on said cell array are performed simultaneously, when the row address does not match the refresh address, while the refresh operation is inhibited and the write operation is performed when the row address matches the refresh address;

comparing the write address held in said address holding circuit with an externally supplied read address; and

controlling so that data from said cell array is read and output to the outside of said semiconductor memory device, when the write address does not match the read address, while data held in said data holding circuit is read and output to said outside of said semiconductor memory device, when the write address matches the read address.

45. The method according to claim 44, further comprising the steps of:

comparing the externally supplied read address with the refresh address; and

performing control so that the refresh operation on said cell array selected by the refresh address and reading of data from said cell array selected by the read address are executed, when the externally supplied

read address does not match the refresh address, while the refresh operation is inhibited and data from said cell array selected by the read address is read, when the externally input read address matches the refresh address.

46. A semiconductor memory device adapted to have an interface compatible with that of a static random access memory device, said semiconductor memory device comprising:

a memory cell array including a plurality of cells, each of which has two port for respective write and read operations and needs a refresh operation to hold data stored therein;

an address holding circuit for holding an externally input address signal;

a refresh address generation circuit for generating a refresh address signal; and

a comparator circuit for comparing the refresh address signal output from said refresh address generation circuit with the input address signal held in said address holding circuit; and

a control circuit for performing control so that, when the comparison result indicates that the refresh address signal does not match the input address signal, a read or write operation using one of the two ports of the cell associated with said input address signal and a refresh operation using the other of the two ports of the cell associated with said refresh address signal are performed in parallel.